IN THE SPECIFICATION

Please amend the portions of the Specification identified below to read as indicated herein.

Paragraph 0015:

[0015] ~~Fig. 7 is depicts~~ Figs. 7(a) and 7(b) depict an estimation of diffusion and perimeter of a standard cell of the present teachings;

Paragraph 0019:

[0019] Fig. 11 ~~is an exemplary a tabular listing of~~ depicts a table of exemplary data.

Paragraph 0032:

[0032] Figs. 5(a) and 5(b) illustrate exemplary circuit models in accordance with the teachings herein. A cell may be represented in a number of ways, such as but not limited, a netlist. ~~A pre-layout representation of a cell provides a pre-layout representation of a cell. The~~ A pre-layout representation may be selected from a wide variety of possibilities such as a spice netlist, a BDD-based transistor structure representation, a pre-layout structural representation like stick diagram, etc.

Paragraph 0052:

[0052] Figs. 7(a) and 7(b) depict an estimation of diffusion and perimeter of a standard cell. It is important to estimate the diffusion area and perimeter of the transistors. Given the width *w* and height *h* of the diffusion region of a transistor, the diffusion area A and perimeter P are calculated as follows:

$$A = w * h \tag{9}$$

$$P = 2 * w + 2 * h \tag{10}$$

Paragraph 0058:

[0058] The capacitance C(n) of a net n is estimated by the following equation:

$$C(n) = \alpha \sum_{t \in TDS(n)} |MTS(t)| + \beta \sum_{t \in TG(n)} |MTS(t)| + \gamma \tag{13}$$

where α, β and γ are constants, *TDS(n)* is a set of transistors whose drain or source is connected to a net n, *TG(n)* is a set of transistors whose gate is connected to a ~~net *n* and~~ net *n*, *MTS(t)* is an MTS that includes a transistor *t*, and *|MTS(t)|* is a number of transistors in *MTS(t)*.

Paragraph 0064:

[0064] The results of the experiments demonstrate the effectiveness of the constructive technique for estimation of wiring capacitances. Wiring capacitances critically determine the quality of the constructive estimator due to their increased effects at the deep submicron geometries. Figs. ~~8(a) and 8(b)~~ 9(a) and 9(b) depict scatter plots that compare extracted and estimated wiring capacitances for the cells in the 130nm (Fig. 9(a)) and 90nm (Fig. 9(b)) technologies, respectively. The extracted capacitance values are calculated from lumped C extracted netlists. The three constants α, β and γ of Equation (13) for these technologies are calculated by multiple regression analyses. This data shows the excellent correlation achieved by the wiring capacitance estimation technique of the present teachings.

Paragraph 0067:

[0067] Fig. 11 depicts a table, i.e., Table 3, of exemplary data. Table 3 demonstrates the effectiveness of the estimators on overall cell timing for the two standard cell libraries under consideration. It is noted that each of the four cell delays (e.g., cell rise, cell fall, transition rise, and transition fall) were measured in the experiment documented by Table 3 ~~(Fig. 11)~~. Columns 1, 2 and 3 list the feature size of the library, the number of cells used in this experiment and the number of wires whose capacitances are estimated in this experiment, respectively. The remainder of the columns compare the quality of the cell timing for each of the proposed techniques. The estimated value for a characteristic of the cell (e.g., cell timing) is accurate to within about 5 percent of a post-layout value of the characteristic. For example, for the 90nm technology library, if no estimation was used, the average of the absolute differences in timing is ~~8.85%~~ 8.81% and a standard deviation of ~~4.08%~~ 4.80%. The statistical approach produces an average absolute difference of 4.10% and a standard deviation of 3.35%. It is noted that the best results are obtained by the constructive estimator, with an average absolute difference of 1.52% and a standard deviation of 1.40%.